

Claims

What is claimed is:

1. A method of forming a semiconductor structure in a semiconductor wafer, the method comprising the steps of:

5 forming an epitaxial layer on at least a portion of a semiconductor substrate of a first conductivity type;

forming at least one trench through the epitaxial layer to at least partially expose the substrate;

10 doping at least one or more sidewalls of the at least one trench with an impurity of a known concentration level so as to form a low-resistance electrical path between an upper surface of the epitaxial layer and the substrate; and

substantially filling the at least one trench with a filler material.

2. The method of claim 1, further comprising the steps of:

15 polishing the upper surface of the epitaxial layer so that the upper surface of the epitaxial layer is substantially planar; and

forming an insulating layer on at least a portion of the upper surface of the semiconductor wafer.

3. The method of claim 1, wherein the step of forming the at least one trench comprises: forming an insulating layer on at least a portion of the epitaxial layer;

20 forming at least one opening in the insulating layer corresponding to the at least trench; and

etching through the epitaxial layer to at least partially expose the substrate.

4. The method of claim 1, wherein the at least one trench comprises a v-groove.

5. The method of claim 1, wherein the step of doping at least one or more sidewalls of the at least one trench with an impurity comprises:

cleaning the sidewalls of the at least one trench to substantially remove any organic material in the at least one trench;

5 predepositing the impurity on at least one or more sidewalls of the at least one trench;

and

driving in the impurity.

6. The method of claim 5, wherein the impurity comprises boron.

7. The method of claim 5, wherein the step of driving in the impurity comprises heating
10 the semiconductor wafer for a predetermined period of time.

8. The method of claim 7, wherein the step of heating the semiconductor wafer comprises heating the semiconductor wafer at a temperature in a range of about 900 degrees Celsius to about 1200 degrees Celsius for a duration of about one hour.

9. The method of claim 5, wherein the step of predepositing the impurity on at least one
15 or more sidewalls of the at least one trench comprises growing an impurity-rich oxide on at least one or more sidewalls of the at least one trench.

10. The method of claim 1, wherein the step of substantially filling the at least one trench comprises depositing a semiconductor material in the at least one trench so as to substantially fill the trench.

20 11. The method of claim 1, wherein the filler material comprises polysilicon material.

12. The method of claim 1, further comprising the step of forming at least one insulating layer on at least a portion of the epitaxial layer.

13. The method of claim 1, further comprising the step of:
forming an active device in the epitaxial layer proximate the upper surface of the epitaxial layer, the active device being in electrical connection with a first end of the at least one trench, a second end of the at least trench being electrically connected to the substrate.

14. The method of claim 13, wherein the active device comprises a metal-oxide-semiconductor device.

15. The method of claim 1, further comprising the steps of:
forming an insulating layer on at least a portion of the upper surface of the epitaxial layer;
forming a gate on at least a portion of the insulating layer;
forming first and second source/drain regions of a second conductivity type in the epitaxial layer proximate the upper surface of the epitaxial layer, the first source/drain region being spaced laterally from the second source/drain region, the gate being formed at least partially between the first and second source/drain regions, the first source/drain region being electrically connected to a first end of the at least one trench and a second end of the at least one trench being electrically connected to the substrate.

16. The method of claim 1, wherein the step of forming at least one trench comprises forming at least two trenches through the epitaxial layer to at least partially expose the substrate, the at least two trenches being spaced about five microns apart relative to one another.

17. The method of claim 1, wherein the at least one trench is formed about one to two microns in width.

18. A semiconductor structure, comprising:

a substrate of a first conductivity type;

an epitaxial layer formed on at least a portion of the substrate; and

at least one trench formed through epitaxial layer and at least partially exposing the

substrate, the at least one trench providing a substantially low-resistance electrical path between an upper surface of the epitaxial layer and the substrate, the at least one trench being formed comprising the steps of: (i) forming at least one opening through the epitaxial layer to expose at least a portion of the substrate, the at least one opening corresponding to the at least one trench; (ii) doping at least one or more sidewalls of the at least one opening with an impurity of a known concentration level; and (iii) substantially filling the at least one opening with a filler material.

19. The semiconductor structure of claim 18, further comprising at least one active device formed in the epitaxial layer proximate the upper surface of the epitaxial layer, the at least one active device being electrically connected to a first end of the at least one trench, a second end of the at least one trench being electrically connected to the substrate.

20. The semiconductor structure of claim 19, wherein the at least one active device comprises a metal-oxide-semiconductor (MOS) device, the MOS device including first and second source/drain regions and a gate formed above the first and second source/drain regions and proximate the upper surface of the epitaxial layer, the first and second source/drain regions being formed in the epitaxial layer proximate the upper surface of the epitaxial layer and spaced apart laterally relative to one another, the gate being at least partially between the first and second source/drain regions, the first source/drain region being electrically connected to the first end of the at least one trench.

21. The semiconductor structure of claim 20, wherein the at least one active device comprises a laterally-diffused MOS (LDMOS) device, the first source/drain region comprising a source region of the device and the second source/drain region comprising a drain region of the device.

5 22. A metal-oxide-semiconductor device, comprising:
 a substrate;
 an epitaxial layer of a first conductivity type formed on at least a portion of the
 substrate;
 a first source/drain region of a second conductivity type formed in the epitaxial layer
 10 proximate an upper surface of the epitaxial layer;
 a second source/drain region of the second conductivity type formed in the epitaxial
 layer proximate the upper surface of the epitaxial layer and spaced laterally from the first
 source/drain region;
 a gate formed above the epitaxial layer proximate the upper surface of the epitaxial
 15 layer and at least partially between the first and second source/drain regions; and
 at least one trench formed in the epitaxial layer, a first end of the at least one trench
 being electrically connected to the first source/drain region at a second end of the at least one trench
 being electrically connected to the substrate, the at least one trench being formed comprising the
 steps of: (i) forming at least one opening through the epitaxial layer to expose at least a portion of
 20 the substrate, the at least one opening corresponding to the at least one trench; (ii) doping at least one
 or more sidewalls of the at least one opening with an impurity of a known concentration level; and
 (iii) substantially filling the at least one opening with a filler material.